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EXAMINER	
YU, HENRY W	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/500,205	HEIZMANN ET AL.	
	Examiner	Art Unit	
	Henry Yu	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6,9,and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,9,and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/03/2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

INFORMATION CONCERNING RESPONSES

Response to Amendment

1. This Office Action is in response to applicant's communication filed August 3, 2007, in response to PTO Office Action mailed May 3, 2007. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, **claims 2-3, 5, 7-8, and 10** have been cancelled, and **claims 1, 4, 6, 9, and 12** has been amended. As a result, **claims 1, 4, 6, 9, and 11-13** are now pending in this application.

3. The objections to the drawings and specification have been withdrawn due to the amendment filed August 3, 2007.

Response to Arguments

4. Applicant's arguments filed on August 3, 2007, in response to the office action mailed May 3, 2007, have been fully considered and are not persuasive.

Applicant argued that Louie et al. (Patent Number US 4,547,849) does not anticipate "*the start signal is transmitted on the control line with a rising or falling edge of a system clock signal during a phase of a clock signal on the clock line and the transfer signal is transmitted on the control line in a phase where no clock signal is present on the clock line.*" However, Louie et al. discloses "*the start signal is transmitted on the control line with a rising or falling edge of a system clock signal during a phase of a clock signal on the clock line*" in FIG. 3-4, where several signals that relate to data

transfer, particularly the COREQ, READY#, and BHE#/LOCK# signals are closely related to the rising and falling of the CLK (or clock) signal, particularly during signal changes. As for "*the transfer signal is transmitted on the control line in a phase where no clock signal is present on the clock line*," there are instances where the COACK# (a signal that is used when the master microprocessor acknowledges the request of the slave microprocessor at the time that it begins the corresponding Data Channel transactions **(Column 24, lines 10-17)**) signal remains high during periods where the CLK signal is low or not present on the clock line (e.g. span '5' of the COACK# signal).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 4, 6, and 9** rejected under 35 U.S.C. 103(a) as being unpatentable over Louie et al. (Patent Number US 4,547,849) in view of Poulis et al. (Patent Number US 6,128,311).

As per **claim 1**, Louie et al. discloses "*the method for setting an operating parameter in a peripheral IC* ***(coprocessor; FIG.1, item 207)*** *comprising: transmitting an operating parameter* ***(data and predetermined address corresponding to said I/O address)*** *from a central IC* ***(microprocessor; FIG. 1, combination of items 200, 202,***

204, 206) *via a bus connection to the peripheral IC* ***(coprocessor; FIG.1, item 207)****, buffering the operating parameter in a preregister* ***(data buffer register and I/O address register; FIG. 6, items 480 and 472 respectively)*** *of the peripheral IC with a current operating parameter stored in a working register* ***(the microprocessor monitors the status of the coprocessor through signals such as BUSY# and ERROR#, which indicate current condition of the coprocessor before transfer)****, sending a transfer signal* ***(COACK# is activated, where the master microprocessor acknowledges the request of the slave microprocessor at the time that it begins the corresponding Data Channel transactions; Column 24, lines 10-17)*** *from the central IC via the bus connection to the peripheral IC* ***(coprocessor; FIG. 1, item 207; Column 7, Table I)****, transferring the buffered operating parameter to said working register if said transfer signal has been received* ***(Column 28, lines 16-25)****, wherein the bus connection is a serial bus connection with a data line, a control line* ***(COREQ and COACK#)****, and a clock line* ***(coprocessor; FIG. 1, item 207; Column 7, Table I)****."*

Louie et al. also discloses "*signaling start of a data transmission* ***(D15-D0)*** *from the central IC* ***(microprocessor; FIG. 1, combination of items 200, 202, 204, 206)*** *to the peripheral IC* ***(coprocessor; FIG. 1, item 207)*** *as well as the transfer signal via said control line* ***(COREQ and COACK#; FIG. 3)****, in which method the start signal is transmitted on the control line with a rising or falling edge of a system clock signal during a phase of a clock signal on the clock line* ***(FIG. 3-4)*** *and the transfer signal* ***(COACK#)*** *is transmitted on the control line in a phase where no clock signal is present*

on the clock line ***(there are particular instances where the COACK# signal is asserted while the CLK signal is low (e.g. span '5' of the COACK# signal; FIG. 3)***."

Though Louie et al. discloses "*the bus connection is a…bus connection with a data line, a control line* ***(COREQ and COACK#)*** *and a clock line, and the transfer signal is transmitted via the control line to the peripheral IC* ***(coprocessor; FIG. 1, item 207; Column 7, Table I)***," Louie et al. does not explicitly disclose the use of serial bus interfacing, which is disclosed by Poulis et al. **(Abstract, lines 1-14)**.

Louie et al. and Poulis et al. are analogous art in that both relate to IC circuits, especially in connection and interface.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by Louie et al. to use a serial bus connection between the processors/IC components as disclosed by Poulis et al.

The motivation for doing so is because Poulis et al. notes that several small-form interfaces can not accommodate parallel communications interfaces, given the plurality of signals that must be present at the same time for parallel communications interfaces. Poulis et al. discloses this as a small-form interface (in this example PCMCIA) **[may dictate the size and hence the capacity of the universal connector, the remaining pins available on the universal connector for interfacing to an external module may be limited thereby prohibiting a parallel interface (Column 4, lines 14-17)]**. On the other hand, serial communications by definition sends all bits sequentially over a single communication channel. With fewer channels needed, one not only can utilize

small-form interfaces that might otherwise preclude the use of parallel communications interface but also simplify the circuit paths between devices/components.

As per **claim 4**, the combination of Louie et al. and Poulis et al. discloses "*the method*" (*see rejection to **claim 1** above*). Louie et al. further discloses "*transferring the register write address **(A23-AO; Column 7, Table I)** for writing to the preregister **(buffer)** in the peripheral IC **(coprocessor)** on the data line ahead of the operating parameter **(data; FIG. 3; Column 28, lines 3-8 and lines 16-25)***." It should also be noted that the idea of transmitting address and data over the same line/bus is inherent in the definition of a serial bus (the use of which is disclosed by Poulis et al. with the motivation also shown for **claim 2**), which only contains a single line for transmission.

As per **claim 6**, the limitations are similar to those disclosed in **claim 1** above. Hence, this claim has been rejected accordingly.

As per **claim 9**, the limitations are similar to those disclosed in **claim 4** above. Hence, this claim has been rejected accordingly.

7. **Claims 11-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Louie et al. (Patent Number US 4,547,849) and Poulis et al. (Patent Number US 6,128,311) in view of Adams et al. (Patent Number US 7,120,427 B1).

As per **claim 11**, the combination of Louie et al. and Poulis et al. discloses the "*device*" (*see rejection to **claims 1 and 6** above, which also includes motivation to combine*). However, the combination of Louie et al. and Poulis et al. does not disclose that "*the peripheral IC relates to a front-end IC for a communication arrangement for wireless data transmission and the central IC relates to a signal processing device, with*

means for modulation or demodulation of the mixed RF input signal and for further signal processing in baseband."

Adams et al. discloses "*the peripheral IC* ***(radio integrated circuit)*** *relates to a front-end IC for a communication arrangement for wireless data transmission* ***(wireless transceiver)*** *and the central IC relates to a signal processing device* ***(receive signal processor and transmit processor, which are located in a modem; Column 5, lines 1-8 and lines 20-24)****, with means for modulation or demodulation* ***(Column 5, lines 1-8 and lines 20-24)*** *of the mixed RF input signal* ***(RF transceiver; Column 4, line 44)*** *and for further signal processing in baseband* ***(Column 4, lines 58-67; Column 17, lines 59-63)***."

Louie et al., Poulis et al., and Adams et al. are analogous art in that both relate to IC circuits, especially in the setting and transfer of data/parameters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by the combination of Louie et al. and Poulis et al. to include components that focus on wireless communication and digital signal processing as disclosed by Adams et al.

The motivation for doing so is because Adams et al. notes that **[different radio applications require a different level of performance, and different levels of performance (Column 1, lines 54-55)]**. In such instances, it would be easier to have a wireless system that is configurable through variable parameters and settings rather than have hard-coded parameters and settings with regards to the appropriate conditions.

As per **claim 12**, the combination of Louie et al., Poulis et al., and Adams et al. discloses the "*device*" (*see rejection to **claim 11** above*). Adams et al. further discloses "*the operating parameter relates to a gain setting for a receive gain in the front-end IC **(gain settings...are set; Column 17, lines 35-39)***."

As per **claim 13**, the combination of Louie et al. and Poulis et al. discloses the "*device*" (*see rejection to **claims 1 and 6** above, which also includes motivation to combine*). However, the combination of Louie et al. and Poulis et al. does not disclose that the "*device is configured as a send and receive device for wireless data transmission in accordance with the HIPERLAN2 standard.*"

Adams et al. discloses "*device is configured as a send and receive device for wireless data transmission **(RF transceiver)** in accordance with the HIPERLAN2 standard **(Column 19, lines 20-30)***."

Louie et al., Poulis et al., and Adams et al. are analogous art in that both relate to IC circuits, especially in the setting and transfer of data/parameters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device as disclosed by the combination of Louie et al. and Poulis et al. to work within a device that handles wireless communication using the HIPERLAN2 standard as disclosed by Adams et al.

The motivation for doing so is because Adams et al. notes that **[different radio applications require a different level of performance, and different levels of performance (Column 1, lines 54-55)]**, and that wireless is becoming more widespread along with the many wireless protocols that are available **(Column 2, lines**

4-5). At the same time, Louie et al. deals with the basic principles of transferring and setting data and parameters between different IC circuits (this can also apply to different sections of a single IC circuit). In such instances, it would be easier to have a wireless system that is configurable through variable parameters and settings rather than have hard-coded parameters and settings with regards to the appropriate conditions.

CONCLUDING REMARKS

Conclusions

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Yu whose telephone number is (571) 272-9779. The examiner can normally be reached on Monday to Friday, 8:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

October 2, 2007
HY

Henry Yu
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KIM HUYNH
SUPERVISORY PATENT EXAMINER
10/15/07